

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of: Fabrice LETERTRE et al.	Confirmation No.: 9120
Patent No.: 7,122,095 B2	Application No.: 10/800,252
Patent Date: October 17, 2006	Filing Date: March 11, 2004
For: METHODS FOR FORMING AN ASSEMBLY FOR TRANSFER OF A USEFUL LAYER	Attorney Docket No.: 4717-10400

**REQUEST FOR CERTIFICATE OF CORRECTION  
UNDER 37 C.F.R. §§ 1.322 and 1.323**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Patentees hereby respectfully request the issuance of a Certificate of Correction in connection with the above-identified patent. The corrections are listed on the attached Form PTO-1050. The corrections requested are as follows:

**Title Page:**

Item (56) **References Cited**, OTHER PUBLICATIONS, S. Kodama et al. reference, change "Gated Gabricated" to -- Gates Fabricated --; and delete "vol. 241ga, p. 434-435 (19099)" and insert -- Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, Japan (1999), pp. 434-435. --.

**Column 6:**

Line 37 (claim 14, line 1), after "The method of claim **12**" delete "wherein". Support for this change appears in the Examiner's Amendment attached to the Notice of Allowability mailed April 13, 2006.

**Column 7:**

Line 6 (claim 25, line 2), after "comprises a seed layer for epitaxial" insert -- growth and at least one epitaxial --. Support for this change appears in application claim 30.

The requested changes are to correct errors of a clerical or typographical nature and do not involve changes that would constitute new matter or require reexamination.

A fee of \$100 is believed to be due for this request. Please charge the required fees to Winston & Strawn LLP Deposit Account No. 50-1814. Please issue a Certificate of Correction in due course.

Respectfully submitted,

10/31/06  
Date

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**UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION**

PATENT NO.: 7,122,095 B2  
APPLICATION NO.: 10/800,252  
DATED: Oct. 17, 2006  
INVENTOR(S): Letertre et al.

Page 1 of 1

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page:

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Column 6:

Line 37, after “The method of claim **12**” delete “wherein”.

Column 7:

Line 6, after “comprises a seed layer for epitaxial” insert -- growth and at least one epitaxial --.



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(12) **United States Patent**  
**Letertre et al.**

(10) **Patent No.:** **US 7,122,095 B2**  
(45) **Date of Patent:** **Oct. 17, 2006**

(54) **METHODS FOR FORMING AN ASSEMBLY  
FOR TRANSFER OF A USEFUL LAYER**

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(\*) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 10 days.

(21) Appl. No.: **10/800,252**

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28, 2003.

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**B32B 37/26** (2006.01)  
**B32B 38/10** (2006.01)  
(52) **U.S. Cl.** ..... **156/344**; 156/257; 156/267;  
427/275; 438/458

(58) **Field of Classification Search** ..... 156/344,  
156/584, 257, 267, 288; 438/458; 427/275  
See application file for complete search history.

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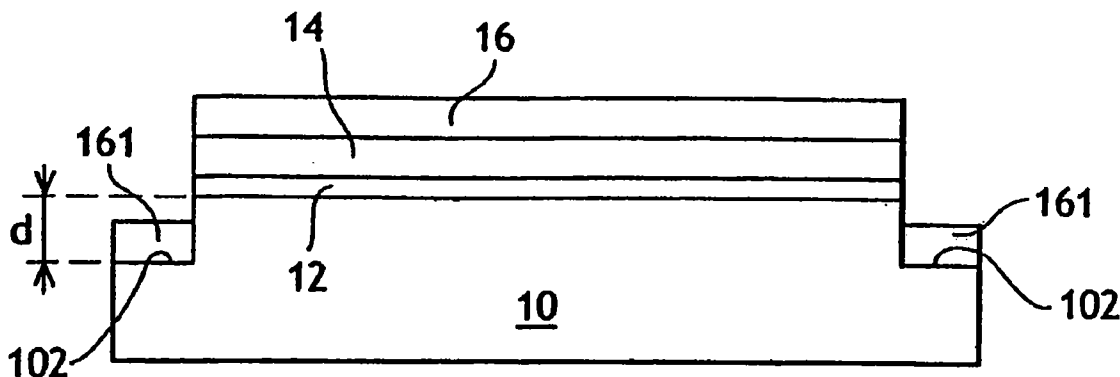
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(57) **ABSTRACT**

Methods for forming an assembly for transfer of a useful layer are described. In an embodiment, the method includes forming a useful layer on a first support having an interface therebetween, and a residual material on a portion of the first support to form the assembly, and processing the assembly to attenuate any bond between the useful layer and the first support caused by the residual material. An implementation of the method includes processing the assembly to remove residual material. In another variation, processing of the assembly includes forming at least one cut or separating channel between a free surface of the useful layer and the interface to separate the useful layer from contact with the residual material. In yet another variation, processing of the assembly includes forming a peripheral recess so that the residual material does not contact the useful layer.

**28 Claims, 2 Drawing Sheets**



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of the residual material 161 deposited on the first support 10, so that at the end of the deposition operation, the peripheral ring 161 does not obstruct and/or does not bond to the detachable interface. Thus, in this case, the ring 161 does not have to be removed. The recess is preferably produced before forming the layers 12 and 14, and in any case before forming all or a portion of the useful layer which may cover the periphery of the first substrate. Preferably, the recess is formed by removing a portion of the first support with a laser beam or by mechanical trimming.

A further approach is shown in FIGS. 5 and 6. In this variation, cuts or channels 18 are formed in the thickness of the useful layer 14, 16, to a depth equal to that of the interface layer 12. These cuts define individual islets or tiles 19. The islets may be square in shape, as shown in FIG. 6, with a size that is preferably in the range of from 1×1 square micrometer ( $\mu\text{m}^2$ ) to 300×300  $\mu\text{m}^2$ . The cuts can be formed either mechanically, for example by using a saw splitting technique, or by using a laser splitting or ion beam splitting technique. The cuts can also be chemically etched by first placing an etching mask on the free surface of the useful layer 14, 16 that allows for a selective geometric attack. Preferably, and in particular to prevent the attack from excavating the walls of the channels too much, a dry or wet etching technique is used. When the useful layer is formed from a seed layer of SiC 14 on which GaN epitaxy is used, argon based ion etching may be used (for further information, see the article "GaN: Processing, Defects and Devices", cited above).

Such an approach avoids reinforcement of the interface between the useful layer and the first support caused by the presence of the peripheral ring 161. In particular, after producing the assembly shown in FIG. 1 channels are formed so that each individualized tile, which is not itself subjected to the reinforcement due to the ring 161, can be detached by force from the support. It should be noted that the force can be a tension, bending or shear stress, or a variety of combinations of such forces.

Clearly, the present invention can be applied to a very wide variety of semiconductor materials. In addition to the example of a layer of nitride developed on silicon carbide on insulator (SiCOI) as described above, the invention can be employed, for example, when transferring a useful silicon layer in which certain methods for fabricating components using CMOS technology on a second insulating support 10 have been carried out. Many other applications are also possible. The skilled person will be able to readily select solutions that are suitable (i.e. choose one of the three approaches described, choose the method of material removal, etc.) as a function of the materials used. In addition, the three approaches of the invention described above can be combined together.

What is claimed is:

1. A method for forming an assembly for transfer of a useful layer comprising:
  - forming a useful layer on a first support having an interface therebetween, and forming a residual material on a portion of the first support to form the assembly; and
  - processing the first support to attenuate bonding between the useful layer and the first support caused by the residual material;
 wherein processing of the first support comprises forming a peripheral recess on the first support so that the residual material does not contact the useful layer.
2. The method of claim 1 wherein the useful layer is weakly bonded to the support to facilitate detachment.

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3. The method of claim 1 wherein the interface is a detachable interface layer provided on the first support before forming the useful layer.

4. The method of claim 1 which further comprises:

affixing a free face of the useful layer to a second support; and

detaching the useful layer at the interface to transfer the useful layer to the second support.

5. The method of claim 4 which further comprises detaching the useful layer by using at least one of tension forces, bending forces and shear stress forces.

6. The method of claim 4 which further comprises directing at least one of a thin blade or a jet of fluid to the interface layer to detach the useful layer.

7. The method of claim 1 wherein processing the first support comprises removing residual material.

8. The method of claim 7 which further comprises removing at least a portion of the first support that is in contact with the removed residual material.

9. The method of claim 7 wherein removing residual material comprises removing at least a portion of a peripheral zone of residual material covering an edge of the interface.

10. The method of claim 9 wherein the peripheral zone is removed by at least one of splitting or etching.

11. The method of claim 10 wherein the peripheral zone is removed by etching and which further comprises masking the useful layer prior to etching.

12. The method of claim 1 wherein the recess is at least one cut or separating channel between a free surface of the useful layer and the interface to separate the useful layer from the residual material.

13. The method of claim 12 wherein the separating channel is cut by using at least one of a saw splitting technique, a laser splitting technique, and an ion beam splitting and masked chemical etching technique.

14. The method of claim 12 wherein which further comprises forming a plurality of cuts or separating channels in the useful layer to form a plurality of useful layer islets.

15. The method of claim 14 which further comprises: affixing free faces of the islets to a second support; and detaching a majority of the islets at the interface.

16. The method of claim 15 which further comprises detaching the islets by using at least one of tension forces, bending forces and shear stress forces.

17. The method of claim 15 wherein the islets are rectangular.

18. The process of claim 1, wherein the width and depth of the peripheral recess is sufficient to accommodate the volume of residual material resulting from formation of the useful layer.

19. The method of claim 1 which further comprises using full wafer epitaxy to deposit at least a portion of the useful layer.

20. The method of claim 19 wherein the useful layer comprises a seed layer for epitaxial growth and at least one epitaxial layer.

21. The method of claim 20 wherein the seed layer is made of at least one of silicon carbide, sapphire, gallium nitride, silicon and aluminum nitride.

22. The method of claim 20 wherein the epitaxial layer is formed from one or more metal nitrides.

23. The method of claim 1 wherein the first support is made from at least one of a semiconductor, a semiconducting or semiconductive carbide, and an insulator material.

24. The method of claim 1 which further comprises providing the interface by at least one of implanting gas

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species, forming a porous layer that can be attacked chemically, and bonding a detachable layer to the first support before forming the useful layer by using a controlled molecular bonding process.

25. The method of claim 1 wherein the useful layer comprises a seed layer for epitaxial layer that forms the residual material. 5

26. The method of claim 25 wherein the seed layer is made of at least one of silicon carbide, sapphire, gallium nitride, silicon and aluminum nitride. 10

27. The method of claim 25 wherein the epitaxial layer is formed from one or more metal nitrides.

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28. A method for forming an assembly for transfer of a useful layer comprising:

forming a peripheral recess on a support; and

forming a useful layer on the support while also forming a residual material on a portion of the support to form the assembly;

wherein the peripheral recess has a width and depth sufficient to accommodate the volume of residual material resulting from formation of the useful layer so that the residual material does not contact the useful layer.

\* \* \* \* \*

growth and at least one epitaxial